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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,120	09/22/2003	Takashi Miyazawa	117244	5416

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EXAMINER	
LUI, DONNA V	
ART UNIT	**PAPER NUMBER**
2629	

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,120	MIYAZAWA, TAKASHI	
	Examiner	Art Unit	
	Donna V. Lui	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *9-12 and 15-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,13,14 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) ___ :e subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/10/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-8, 13-14, and 20 in the reply filed on April 7, 2006 is acknowledged.

2. Claims 9-12 and 15-19 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on April 7, 2006.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

4. **Claims 3-5** are objected to because of the following informalities:

Claims 3, 4, and 5 recite the limitation of having a third, fourth, and fifth transistor respectively when no intermediate transistors are claimed after having a first.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1, 3-8, 13-14, and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Dawson et al. (Patent No.: US 6,229,506 B1) in view of Tsuchida et al. (Pub. No.: US 2002/0196215 A1). Please note the above claim objections pertaining to claims 3-5.

With respect to **Claim 1**, Dawson teaches an electronic circuit *(See figure 2)* comprising: an electronic element *(element 290: OLED)*; a capacitor *(element 280; column 3, lines 50-52)* for accumulating a data signal in a form of an amount of charge; and a first transistor *(element 260; column 3, line 64 to column 4, line 5; column 3, lines 36-39)* whose conduction state is set in accordance with the amount of charge accumulated in the capacitor, the first transistor supplying an amount of current in accordance with the conduction state to the electronic element. Dawson teaches the capacitor being capable of accumulating a data current as the data signal *(See figure 2, element 230: data current)* but does not teach the capacitor being capable of accumulating a data voltage as the data signal.

Tsuchida teaches a data line *(See figure 1, element 2)* that includes constant voltage sources *(V1, V2, ..., V256)* and constant current sources *(CB1, CB2, ..., CB256)* and driving switches *(D1, D2, ..., D256)* for selection of the source *([0029], lines 1-3)*.

The electronic circuit of Dawson is modified by Tsuchida in such a way that the data line *(See figure 2, element 220)* of Dawson is replaced by the data driving circuit *(See figure 1, element 2)* of Tsuchida so that the modification results in the capacitor being capable of

accumulating a data voltage as the data signal dependent on the driving switches for selecting either a constant voltage source or a constant current source.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use the data line of Tsuchida to the electronic circuit of Dawson so as to provide a display that requires a shorter time to emit light with a desired instantaneous brightness and has less variation in instantaneous brightness during a scanning period *(Tsuchida: [0010])*.

With respect to **Claim 3**, Dawson teaches a transistor *(See figure 2, element 240)* being provided between a gate and a drain of the first transistor *(element 260)*.

With respect to **Claim 4**, Dawson teaches a transistor *(See figure 2, element 250; column 3, lines 36-39 and lines 55-57)* to determine a timing to start or stop supply of the current to the electronic element after the conduction state of the first transistor *(element 260)* is set according to the data signal.

With respect to **Claim 5**, Dawson teaches an electronic circuit *(See figure 2)* comprising: an electronic element *(element 290: OLED)*; a capacitor *(element 280; column 3, lines 50-52)* that is capable of accumulating a data current as a data signal in a form of an amount of charge; a first transistor *(element 260; column 3, line 64 to column 4, line 5; column 3, lines 36-39)* whose conduction state is set in accordance with the amount of charge accumulated in the capacitor, the first transistor supplying an amount of current in accordance with the conduction state to the electronic element; and a fifth transistor *(element 270; column 3, lines 20-22 and lines 44-52)* for

resetting the amount of charge held in the capacitor to a predetermined state when the fifth transistor is turned on. Dawson teaches the capacitor being capable of accumulating a data current as the data signal *(See figure 2, element 230: data current)* but does not teach the capacitor being capable of accumulating a data voltage as the data signal.

Tsuchida teaches a data line *(See figure 1, element 2)* that includes constant voltage sources *(V1, V2, ..., V256)* and constant current sources *(CB1, CB2, ..., CB256)* and driving switches *(D1, D2, ..., D256)* for selection of the source *([0029], lines 1-3)*.

The electronic circuit of Dawson is modified by Tsuchida in such a way that the data line *(See figure 2, element 220)* of Dawson is replaced by the data driving circuit *(See figure 1, element 2)* of Tsuchida so that the modification results in the capacitor being capable of accumulating a data voltage as the data signal dependent on the driving switches for selecting either a constant voltage source or a constant current source.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use the data line of Tsuchida to the electronic circuit of Dawson so as to provide a display that requires a shorter time to emit light with a desired instantaneous brightness and has less variation in instantaneous brightness during a scanning period *(Tsuchida: [0010])*.

With respect to **Claim 6**, Dawson teaches an electro-optical device *(See figure 1)* including a plurality of scanning lines *(130a, 130b, ...)*, a plurality of data lines *(140a, 140b, ...)*, and a plurality of unit circuits *(See figure 2)*. Dawson does not teach the electro-optical device comprising: a data-voltage outputting circuit that outputs binary data voltages to the plurality of

unit circuits via the plurality of data lines; and a data-current outputting circuit that outputs data currents to the plurality of unit circuits via the plurality of data lines.

Tsuchida teaches a data line driving circuit *(See figure 1, element 2)* that comprises a data-voltage outputting circuit *(V1, V2, ..., V256: note that the circuit outputs binary data voltages since the levels are either 0 or 1 equivalent to 0V or a certain voltage level)* that outputs binary data voltages to the plurality of unit circuits via the plurality of data lines; and a data-current outputting circuit *(CB1, CB2, ..., CB256)* that outputs data currents to the plurality of unit circuits via the plurality of data lines. Tsuchida teaches the use of driving switches *(D1, D2, ..., D256)* for selection of the either the constant voltage source or constant current source *([0029], lines 1-3)*.

The electro-optical device of Dawson is modified by Tsuchida in such a way that the data line *(See figure 2, element 220)* of Dawson is replaced by the data line driving circuit *(See figure 1, element 2)* of Tsuchida so that the modification results in a data-voltage outputting circuit that outputs binary data voltages to the plurality of unit circuits via the plurality of data lines; and a data-current outputting circuit that outputs data currents to the plurality of unit circuits via the plurality of data lines through the use of driving switches for selection of the source. .

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use the data line of Tsuchida to the electro-optical device of Dawson so as to provide a display that requires a shorter time to emit light with a desired instantaneous brightness and has less variation in instantaneous brightness during a scanning period *(Tsuchida: [0010])*.

With respect to **Claim 7**, Dawson does not teach the data voltages and the data currents being supplied via each of the plurality of data lines.

Tsuchida teaches the data voltages *(See figure 1, V1, V2, ..., V256)* and the data currents *(CB1, CB2, ..., CB256)* being supplied via each of the plurality of data lines *(A1, A2, ..., A256)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use data voltages and the data currents being supplied via each of the plurality of data lines, as taught by Tsuchida to the electro-optical device of Dawson, so as to provide a display that requires a shorter time to emit light with a desired instantaneous brightness and has less variation in instantaneous brightness during a scanning period *(Tsuchida: [0010])*.

With respect to **Claim 8**, Dawson does not teach the data voltages and the data currents being supplied via different data lines of the plurality of data lines, respectively.

Tsuchida teaches the data voltages *(See figure 1, V1, V2, ..., V256)* and the data currents *(CB1, CB2, ..., CB256)* being supplied via different data lines *(A1, A2, ..., A256)* of the plurality of data lines, respectively.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use data voltages and the data currents being supplied via different data lines of the plurality of data lines, respectively, as taught by Tsuchida to the electro-optical device of Dawson, so as to provide a display that requires a shorter time to emit light with a desired instantaneous brightness and has less variation in instantaneous brightness during a scanning period *(Tsuchida: [0010])*.

With respect to **Claim 13**, Dawson teaches the electro-optical elements being EL elements *(See figure 2, element 290: OLED)*.

With respect to **Claim 14**, Dawson teaches each of the EL elements having a light-emitting layer that is composed of an organic material *(See figure 2, element 290: OLED; column 2, lines 60-66)*.

With respect to **Claim 20**, Dawson teaches an electronic apparatus comprising an electro-optical device *(See figures 1 and 2, element 290: OLED)*.

7. **Claim 2** is rejected under 35 U.S.C. 103(a) as being unpatentable over Dawson and Tsuchida, as applied to Claim 1 above, and further in view of Adachi et al. (Pub. No.: US 2003/0058195 A1) and Inoue et al. (Pub. No.: US 2002/0154104 A1).

With respect to **Claim 2**, note the above rejection pertaining to claim 1. Dawson does not teach the data current being a multi-value data current, the data voltage being a binary data voltage, and the multi-value data current and the binary data voltage being supplied to the capacitor via a second transistor. In the above modification of Dawson by Tsuchida, Tsuchida replaces the data line of Dawson by a data driving circuit, such a modification results in data current and data voltage being supplied to the capacitor via switches (driving switches D1, D2, ..., D256). It would have been obvious for a person of ordinary skill in the art at the time the

invention was made to use transistors in place of the driving switches in the electronic circuit of Dawson as modified by Tsuchida, so as to provide higher reliability and faster response time as characteristic of transistors.

Tsuchida does not mention the data current being a multi-value data current and the data voltage being a binary data voltage.

Adachi teaches data current being a multi-value data current *([0033], lines 2-8; [0097])*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use data current being a multi-value data current, as taught by Adachi, to the electronic circuit of Dawson as modified by Tsuchida, so as to be able to increase the number of display gray scale without increasing the number of subframes *([0033], lines 6-8)* and to prevent image quality degradation such as dynamic contouring without increasing power *([0104])*.

Inoue teaches data voltage being a binary data voltage *([0095], lines 3-7)*. It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use data voltage being a binary data voltage, as taught by Inoue, to the electronic circuit of Dawson as modified by Tsuchida and Adachi, so as to provide a high quality tone display *([0185])*.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Oomura (Patent No.: US 6,693,388 B2) is cited to teach a data side drive circuit that has a voltage comparator having a voltage of a reference voltage source Vr as one input and a reference current source Id having luminance information are arranged.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna V. Lui whose telephone number is (571) 272-4920. The examiner can normally be reached on Monday through Friday 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571)272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Donna V Lui
Examiner
Art Unit 2629

AMR A. AWAD
PRIMARY EXAMINER